IN THE CLAIMS

Please rewrite claim 2 as follows:

1. (Cancelled).

2. (Currently Amended) A method for forming a via hole of a semiconductor device comprising:

a step of forming a first step via hole in a laminated structure formed by a copper layer, an etching-stop layer formed on a surface of said copper layer, and an insulation layer formed on a surface of said etching-stop layer, thereby a bottom of said first step via hole is stopped at said etching-stop layer;

a step of forming a second step via hole continuous with said first step via hole in said etching-stop layer, thereby a bottom of said second step via hole reaching at said surface of said copper layer;

a step of cleaning said second step via hole, said step of cleaning including an annealing process for said via ~~hole;~~ hole, said step of cleaning not using an organic gas; and

a step, after said cleaning, of forming a barrier film on said first and second step via holes, by sputtering.

3. (Previously Presented) A method for forming a via hole of a semiconductor device according to claim 2, wherein said annealing process for said via hole is performed at a low oxygen partial pressure.

4. (Original) A method for forming a via hole of a semiconductor device according to claim 3, wherein said step of cleaning said via hole further comprises a step for treating said via hole with an oxygen plasma, before said step of annealing said via hole at a low oxygen partial pressure.

5. (Original) A method for forming a via hole of a semiconductor device according to claim 4, wherein said step of cleaning said via hole further comprises a step for performing wet processing of the via hole after treating said via hole with an oxygen plasma.

6. (Original) A method for forming a via hole of a semiconductor device according to claim 3, wherein said step of annealing said via hole at a low oxygen partial pressure is further performed in a sputtering chamber for said sputtering.

7. (Original) A method for forming a via hole of a semiconductor device according to claim 6, wherein said step for annealing said via hole at a low oxygen partial pressure is further performed immediately before said sputtering.

8. (Original) A method for forming a via hole of a semiconductor device according to claim 7, wherein said semiconductor substrate in the step for annealing said via hole at a low oxygen partial pressure is held in said sputtering chamber at a temperature of 250 °C or greater for at least three minutes before said step of forming a barrier film.

9. (Original) A method for forming a via hole of a semiconductor device according to claim 8, wherein the oxygen partial pressure when said sputtering is performed is 1 Torr or lower.

10. (Original) A method for forming a via hole of a semiconductor device according to claim 8, wherein said step of annealing said via hole at a low oxygen partial pressure is performed in a hydrogen atmosphere.

11. (Original) A method for forming a via hole of a semiconductor device according to claim 10, wherein said step of annealing said via hole at a low oxygen partial pressure is performed in an atmosphere in which hydrogen radicals are supplied.